

## **Design and Analysis of a Novel Low -Power SRAM for high speed vlsi design**

<sup>1</sup>pujari mounika , <sup>2</sup>Mahesh mudavath

<sup>1</sup>PG Scholar, Electronics and Communication Engineering, vaagdevi college of engineering,thimmapoor, waranga, telangana, India.

<sup>2</sup>Assistant Professor, Electronics and Communication Engineering, vaagdevi college of engineering,thimmapoor, waranga, telangana, India.  
mounika496@gmail.com

---

**ABSTRACT:** In this paper we propose a novel design of a low power static random access memory (SRAM) cell for high speed operations. The model adopts the voltage mode method for reducing the voltage swing during the write operation switching activity. Dynamic power dissipation increases when the operating frequency of the SRAM cell increases. In the proposed design we use two voltage sources connected with the Bit line and Bit bar line for reducing the voltage swing during the write “0” or write “1” operation. We use 90 nm CMOS technology with 1 volt of power supply. Simulation is done in Microwind 3.1 by using BSim4 model. Dynamic power for different frequencies is calculated. We compare it with conventional 6-T SRAM cell. The simulation results show that the power dissipation is almost constant even the frequency of the proposed SRAM model increases. This justifies the reduction of the dynamic power dissipation for high frequency CMOS VLSI design.

**KEY WORDS :** CMOS; Dynamic power; SRAM; Voltage Mode; Voltage Swing

---

### **I. INTRODUCTION**

In today's technology advancement world, Reduction of power consumption makes a device more reliable. The need for devices which dissipate minimum amount of power was a major driving force behind the development of CMOS technologies. Consequently, CMOS devices are best known for low power consumption. However, for minimizing the power requirements for a system, by knowing that CMOS devices may use less power than equivalent devices from other technologies does not do enough [1]. For high speed systems, Low power design has become an essential issue in VLSI design [2]. Normally, dynamic power dissipation dominates in most digital systems. Dynamic power dissipation depends on the switching frequency, supply voltage, and the output voltage swing. Reduction in the supply voltage is the most efficient approach to minimize the dynamic power dissipation. Unfortunately, lower supply voltage leads to degradation in performance dramatically [3]. Lower supply voltage decreases the threshold voltage which will increase the sub-threshold current or leakage current hence the static power dissipation increases. Also by Limiting the output voltage swing, dynamic power and delay can be reduced. Various methods can be used for reducing the voltage swing during the switching activities in SRAM design. One of the best techniques is Charge Sharing method. In this technique, by using a charge sharing method the bit-lines voltage swing has been reduced [4]. Another technique called as half swing pulse mode method is also proposed so as to reduce the dynamic power [5]. Hierarchically divided bit-line approach is shown too effective for reducing the active power in SRAMs by reducing bit-line capacitance [6]. Multiple valued techniques are also very useful method for reducing the voltage swing of the output [7, 8]. In this paper a design technique for low power high speed SRAM circuits is proposed. The proposed SRAM cell, unlike the conventional 6T SRAM contains two extra transistors connected with two different voltage sources for reduction in the voltage swing during write operation. It is found that for high frequency of operation, the dynamic power dissipation is almost constant for the proposed SRAM cell.

### **II. DESIGN OF CONVENTIONAL 6T SRAM CELL**

6T SRAM cell each bit in SRAM is stored on four transistors that form two cross coupled inverter. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to storage cell during read and write operation. [1] Access to the cell is enabled by the word line which controls the two access transistor which in term control, whether the cell should be connected to the bit line BL and BL BAR. [2] They are used to transfer data for both read and write operations. An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested

and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. [3, 4]

The 6-T SRAM cell operates as follows:

**(1) For a read operation,** Basic condition is that the strength (drive current) of the pull-down transistor to that of the pass-gate transistor should be sufficiently large. It is called cell Beta ratio. The bit-lines are usually *pre-charged* To a high level (VDD) and then the word-line is selected (pulsed to a high level). On the side of the cell storing a Logical „0“ (*i.e.*, a low Voltage), the bit line is discharged via the pass-gate transistor and pull-down transistor, so that a differential voltage develops between the bit-lines. This differential voltage should be large enough for a sense amplifier to detect the state of the cell. The differential voltage should not be too large, however; otherwise the cross-coupled inverters could flip their state.

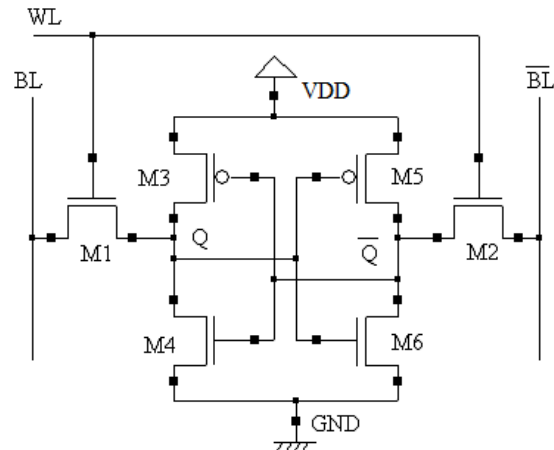


Figure 1. Conventional 6T SRAM Cell.

**(2) For a write operation,** Basic condition is that the ratio of the strength of the pass-gate transistor to that of the pull-up transistor should be sufficiently large. It is called cell *gamma ratio*. The bit-lines are driven to complementary voltage levels via a write driver and then the word-line is selected. On the side of the cell for which the bit-line voltage is logical „0“ (*i.e.*, a low voltage), the internal storage node is discharged through the pass-gate transistor. The cross-coupled inverters raise the voltage on the opposite storage node and latch the cell. The discharging strength of the pass-gate transistor must overcome the restoring strength of the pull-up transistor.

**(3) For a Standby Operation,** Basic condition is that the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two Cross coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as long as they are connected to the supply.

### III. PROPOSED SRAM CELL

In order to improve the performance in the conventional 6T SRAM, we have modified the classical SRAM configuration. The proposed SRAM cell results constant power dissipation with increase in the frequency. In the proposed design we have used two different voltage sources VS1 and VS2 connected to the output of the in3 and in1 line. Two NMOS transistor VT1 and VT2 are connected with input of in3 and in1 line directly to switch ON and switch OFF the power source supply during write “0” and write “1” operations, respectively. The proposed design has been shown in Figure 2. These power supply sources reduce the voltage swing at the output node when write operation is being performed.

**A. Write '0' operation :** During the write '0' operation, in3 line is low and in1 line goes to high. So the transistor VT2 is ON and VT1 OFF condition. Hence the voltage source VS2 leads to decrease the voltage swing at output of the in1 line.

**B. Write '1' operation :** During the write '1' operation, the transistor VT1 is ON and VT2 in the OFF condition, so the voltage source VS1 leads to decreases the voltage swing at the in3 line output. Since decrease in voltage swing dynamic power dissipation is kept almost constant even if increase in the frequency of the SRAM cell. The dynamic power may be expressed as

$$P_{dynamic} = \alpha C V_{dd} V_{swing} f$$

Where,  $C$  = Load capacitance,  $\alpha$ = Activity factor,  $f$ =Clock frequency,  $V_{swing}$  = Voltage swing at output node.

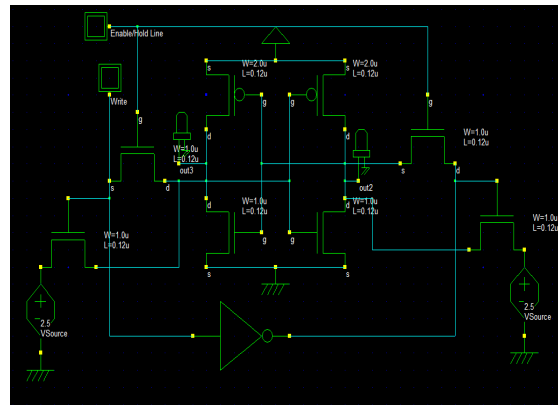
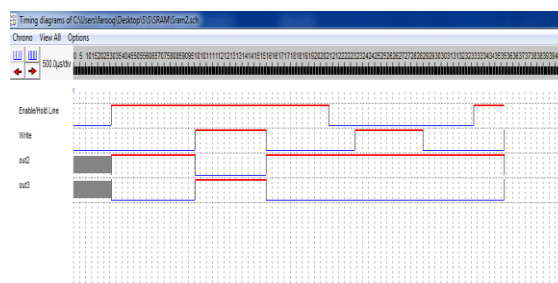


Figure 2. Proposed SRAM Cell

Hence increase in the frequency leads to increase in the dynamic power dissipation as the dynamic power depends upon the operating frequency [10]. In this proposed SRAM model voltage source VS1 and VS2 leads to decrease in the voltage swing during switching activity. With the increase in frequency the switching activity will also be increased but voltage source leads to decrease in its voltage swing simultaneously at the output. Hence at higher frequency the dynamic power dissipation is almost constant. For better performance of SRAM cell, the size of the transistors plays a major role. According to the rule of thumb the width ratio of the transistor T1 and T2 is nearly equal to 1.5 and the width ratio for T2 and T3 is also equal to 1.5. Consequently it is applicable for transistors T4, T5 and T6, respectively

#### IV. RESULTS AND DISCUSSIONS

Here we have given the detailed simulation analysis performed for the proposed SRAM cell. We have seen the performance of the proposed SRAM cell on the power dissipation during write operation. The schematic of proposed SRAM cell is designed and implemented by using DSCH and Microwind. For simulation we are using 1V power supply. The proposed design has been simulated using different foundry size CMOS technology 90nm, 65nm and 45nm respectively for different frequencies. VS1 and VS2 have been taken 0.5 volt during simulation. These simulated results are compared with the conventional 6-T SRAM cell.



#### V. CONCLUSION

In high speed VLSI design dynamic power consumption has become an important issue. In this paper we have analysed the proposed SRAM cell design for low dynamic power consumption by using different foundry size. The proposed SRAM cell has two voltage sources which are used for adjusting the voltage swing during switching. The reduction in voltage swing results a reduction of dynamic power. Dynamic power dissipation for proposed SRAM cell decreases with decrease in foundry size for high speed operations. It can be observed from the simulation that the power dissipation has been decreased from 4.04% to 10.44% by reducing the foundry size from 90nm to 65nm to 45 nm. Though numbers of transistors and area are increased in comparison to conventional SRAM cell but low power dissipation even at very high frequency can easily

overcome the area power trade off. This proposed SRAM cell can be used to provide low power utilization in different high speed handheld devices like laptops, mobile phones, programmable logic devices etc.

### REFERENCES

- [1] A. P. Chandrakasan and R. W. Broderson, "Minimizing power consumption in digital CMOS circuits," Proc. of the IEEE, vol. 83,no.4,pp. 498- 523, April 1995.
- [2] P. K. S. Vasundara, and K. S. Gurumurthy, "Quaternary CMOS Combinational Logic Circuits," IEEE Internatinal Conferece on Information and Multimedia Technology, pp. 538- 542,Dec. 2009.
- [3] B. Ebrahimi, S. Zeinolabedinzadeh, and A. A. Kusha,"Low Standby Power and Robust FinFET Based SRAM Design", IEEE Computer Society Annual Symposium on VLSI, pp. 185-190, Jan 2008.
- [4] Gu Ming, Yang Jun, Xue Jun, "Low power SRAM design using charge sharing technique," 6<sup>th</sup> International Conference On ASIC, ASICON,pp.19-23, Oct.2005.
- [5] K.W. Mai, T. Mori, B. S. Amrutur, R. Ho, B. Wilburn, M. A. Horowitz,I. Fukushi, T. Izawa, and S. Mitarai, "Low power SRAM design using halfswing pulsemode techniques", IEEE J. Solid-State Circuits, Vol.33,no.1, pp. 1659-71, Jan. 1998.
- [6] A. Karandikar,; K. K. Parhi, "Low power SRAM design using hierarchcal divided bit-line approach," International Conference on Computer Design: VLSI in Computers and Processors, ICCD '98, pp.82-88, 5-7 Oct 1998.
- [7] I. Thoidis, D. Sourdris, I. Karafyllidis, A. Thanailakis, and T. Stouritis,"Design Methodology of Multiple-Valued Logic Voltage-Mode Storage Circuits", IEEE Internatinal Symposium on Circuit and System,pp. 125-128, March 1998.
- [8] R. C. G. da Silva, H. Boudinov, L. Carro, "A Novel Voltage-Mode CMOS Quaternary Logic Design", IEEE Transaction on Electron Devices, vol. 53, no. 6, pp. 1480-1483, June 2006.
- [9] Keivan Navi, Roshanak Zabihi, Majid Haghparast, Touraj Nikobin, "A Novel Mixed Mode Current and Dynamic Voltage Full adder", World Applied Sciences Journal, Vol.4,no.2, pp. 289 -294, 2008.

### AUTHORS:



**First Author:** pujari mounika received the B.Tech degree in Electronics and Communication Engineering in the year 2012 from balaji institute of technology and pursuing M.Tech degree in VLSI Design from vaagdevi college of engineering,thimmapoor, waranga, telangana, India. area of interests includes VLSI Design, VLSI, AISC and Signal Processing.



**Second Author:** Mahesh mudavath graduated from Bharath institute of engineering&technology and received his Master degree from CDAC in VLSI DESIGN, mohali, pujab. He is currently working as Assistant Professor in Electronics and Communication Department,vaagdevi college of engineering,thimmapoor, waranga, telangana, India His current research interests include Biomedical Signal Processing, Embedded Systems Design, Virtual Instrumentation and Digital Design.